PCT/KR2004/000000

FIG.1
Background Art

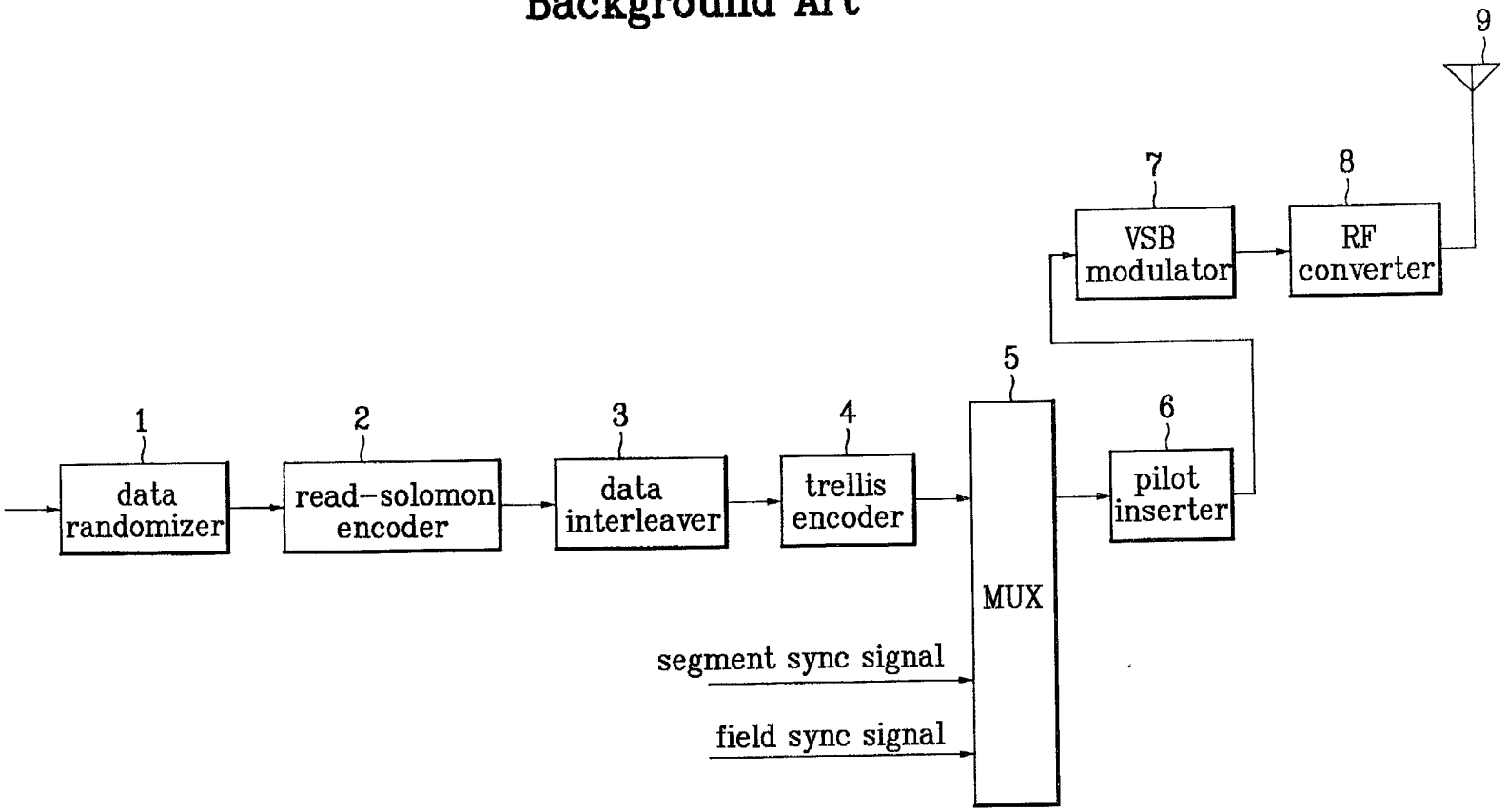


FIG.2
Background Art

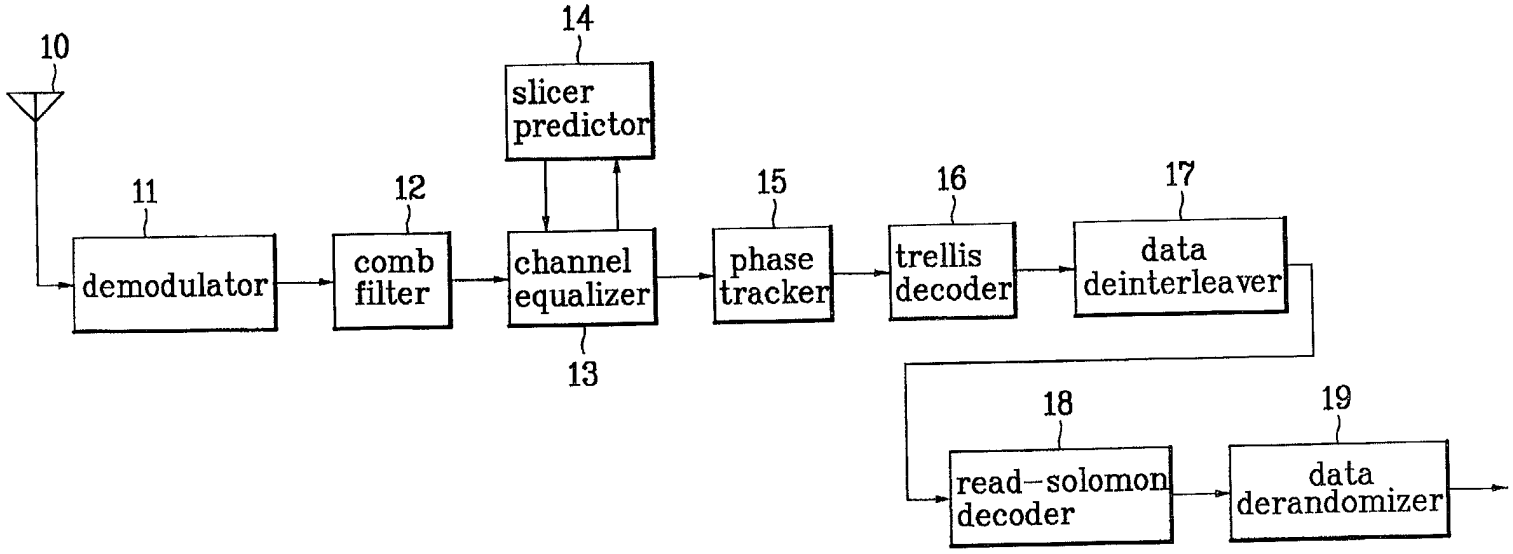


FIG.3

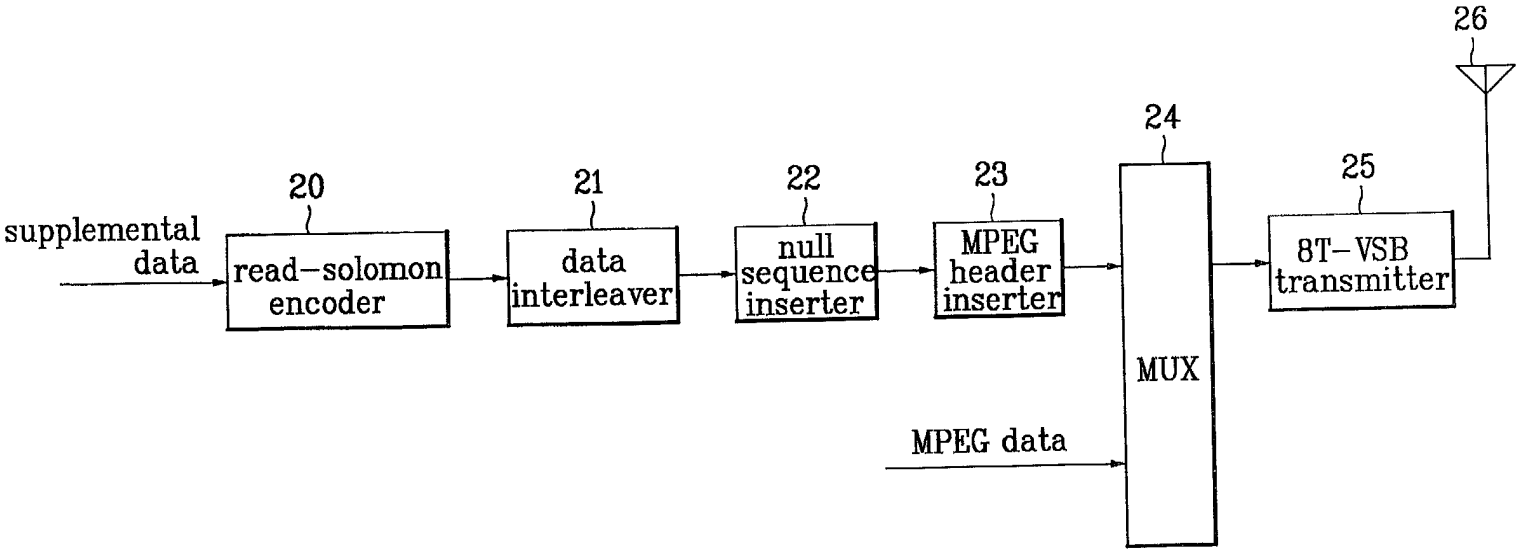
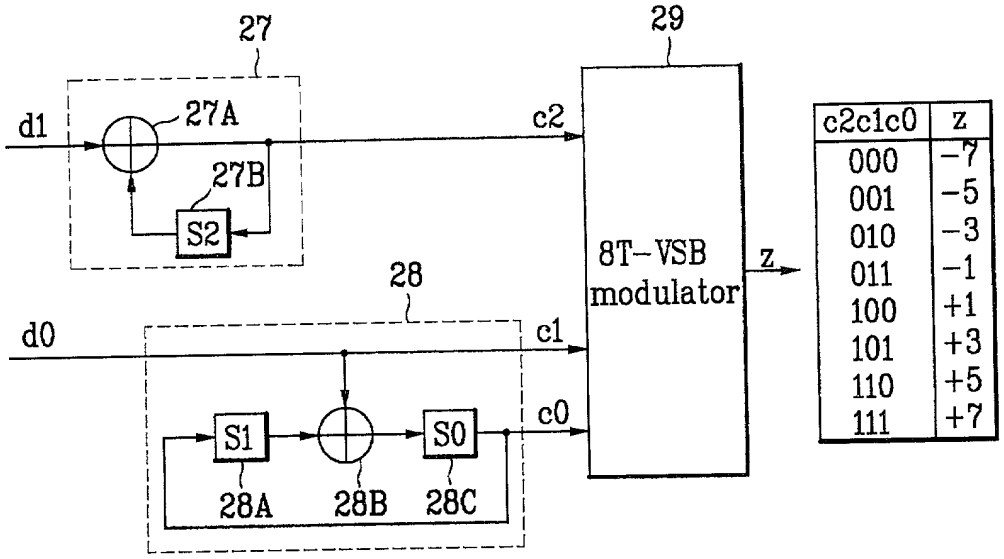

supplemental data
20
read-solomon encoder
21
data interleaver
22
null sequence inserter
23
MPEG header inserter
24
MUX
MPEG data
25
8T-VSB transmitter
26

FIG. 4



c2c1c0	z
000	−7
001	−5
010	−3
011	−1
100	+1
101	+3
110	+5
111	+7

FIG.5

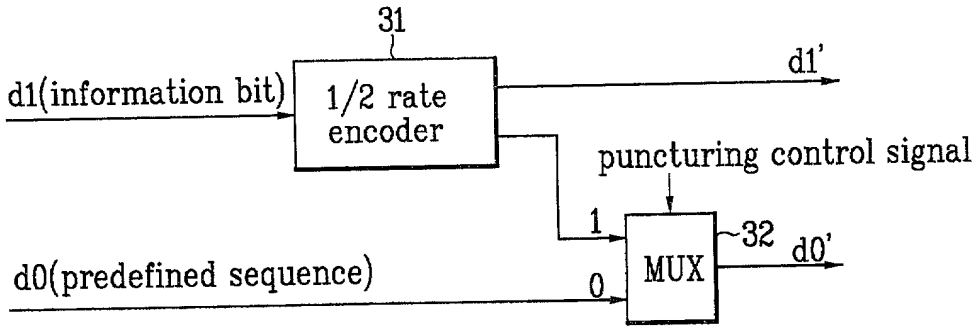
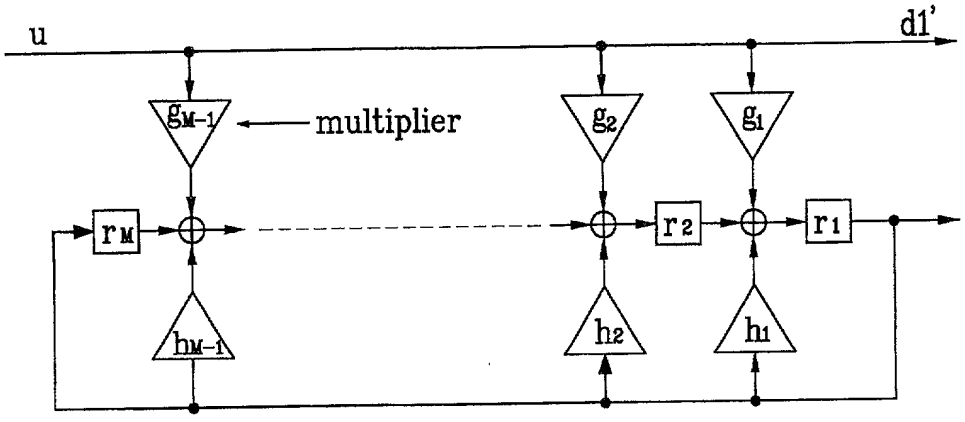


FIG.6



$g_i, h_i \in \{0,1\}, i=1 \ldots M-1$

FIG. 7A

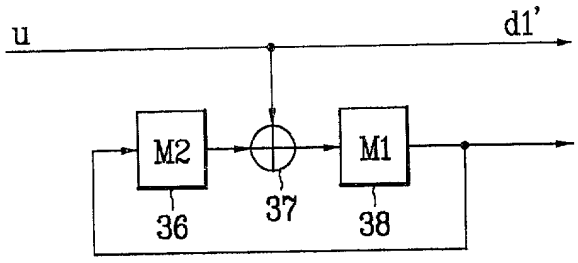


FIG. 7B

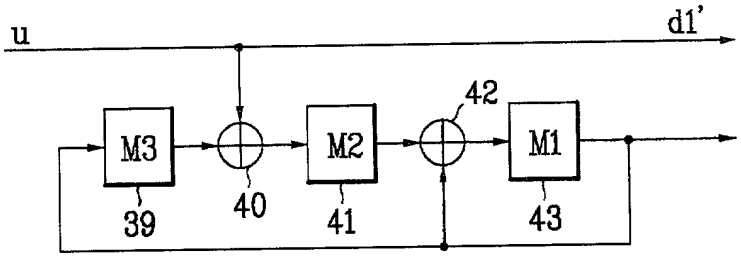


FIG. 7C

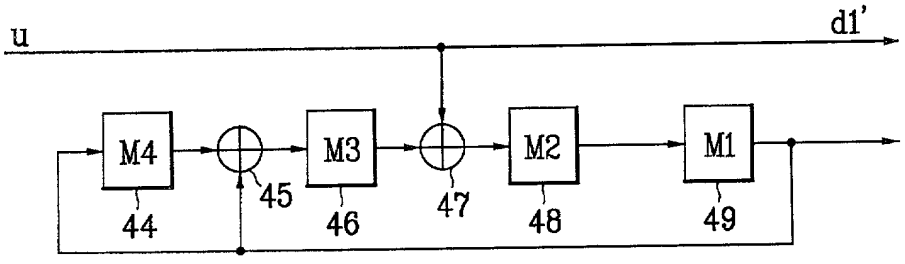


FIG.8

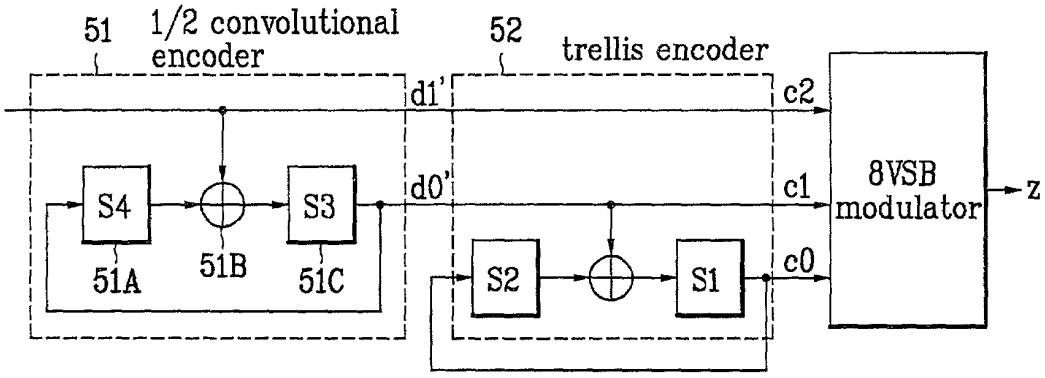

51
1/2 convolutional encoder
52
trellis encoder
d1'
d0'
c2
c1
c0
S4
S3
S2
S1
51A
51B
51C
8VSB modulator
z

FIG.9

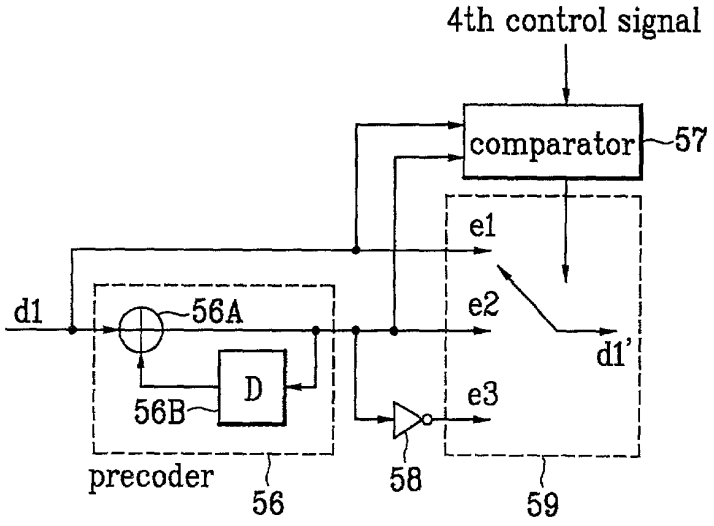
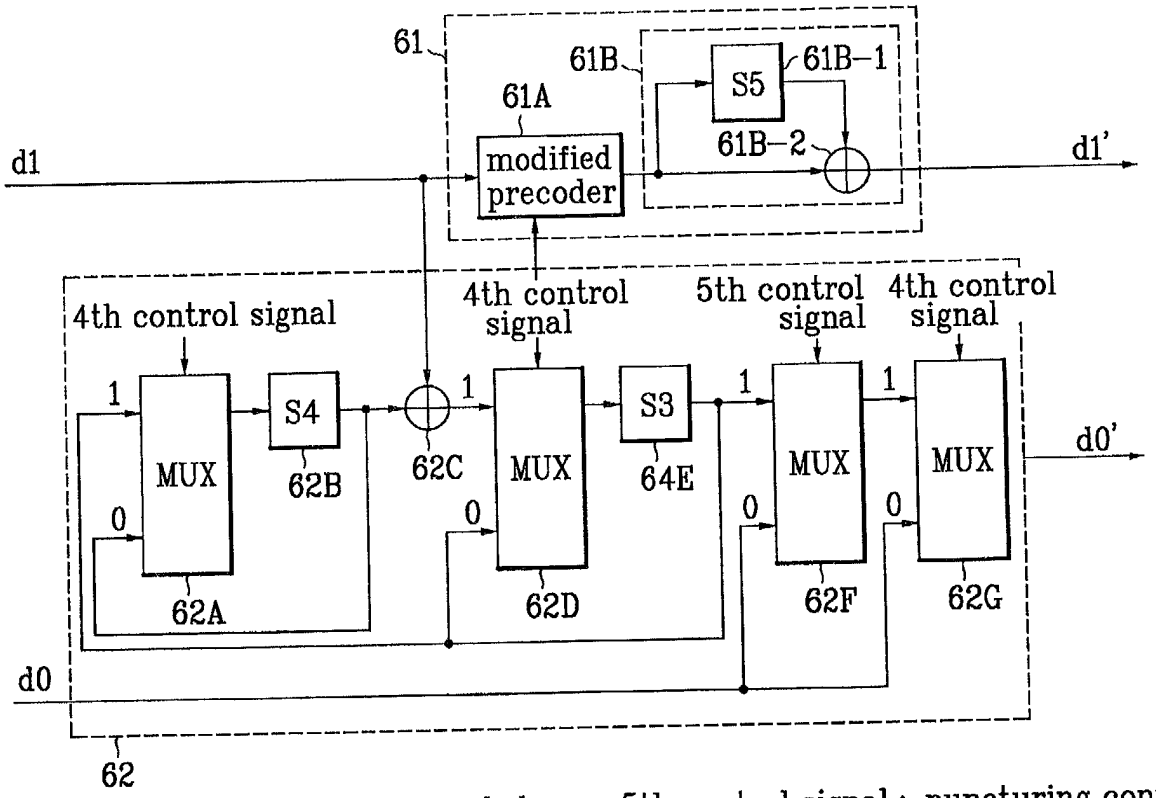

4th control signal
comparator
57
e1
e2
e3
d1
d1'
56A
D
56B
precoder
56
58
59

FIG.10



4th control signal : supplemental data symbol indicating signal
(1) : supplemental data symbol including null bit
(0) : all others

5th control signal : puncturing control signal
(1) : transmit encoded parity bit
(0) : transmit predefined sequence

PATENT PENDING

FIG.11

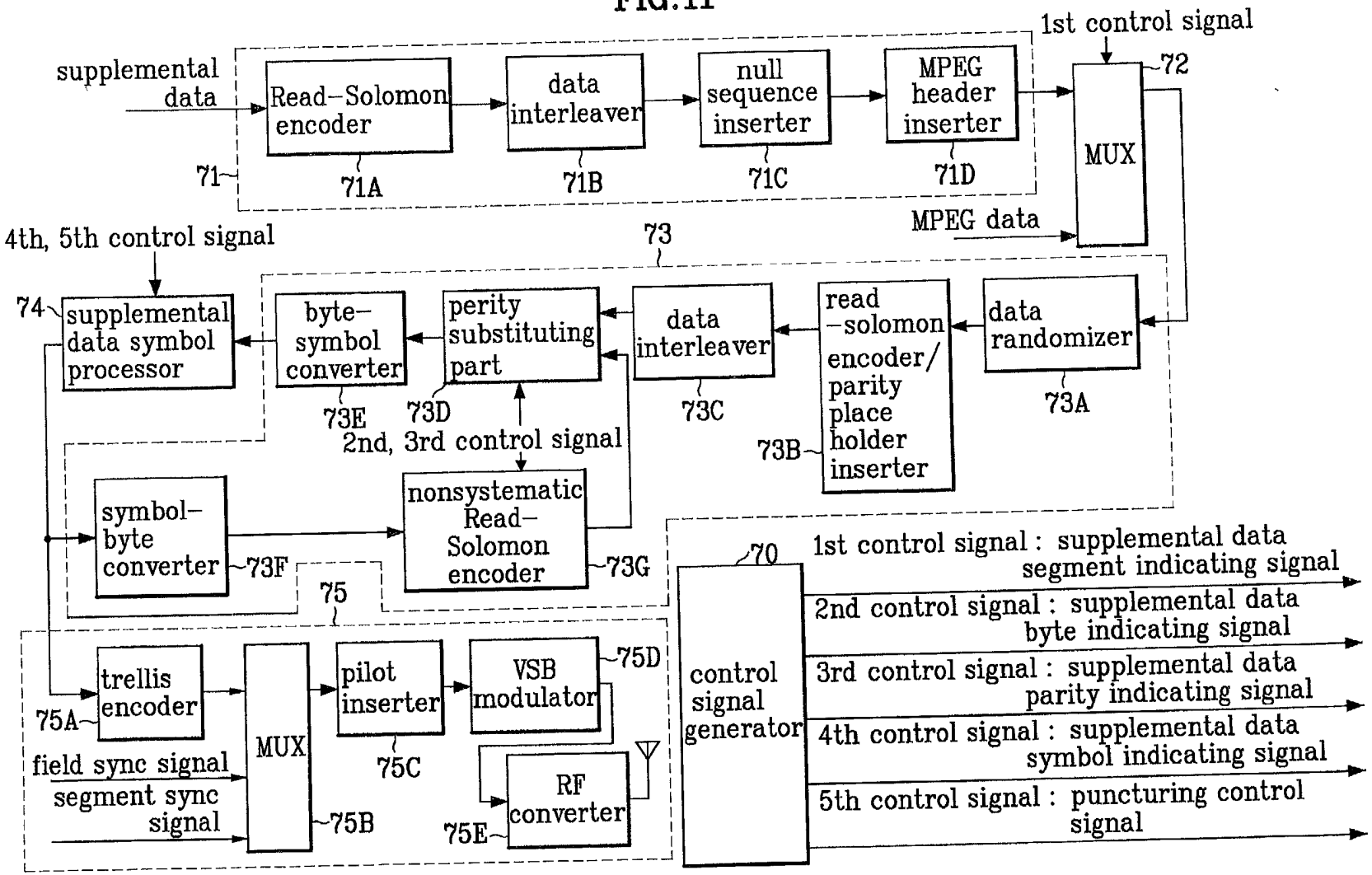


FIG.12

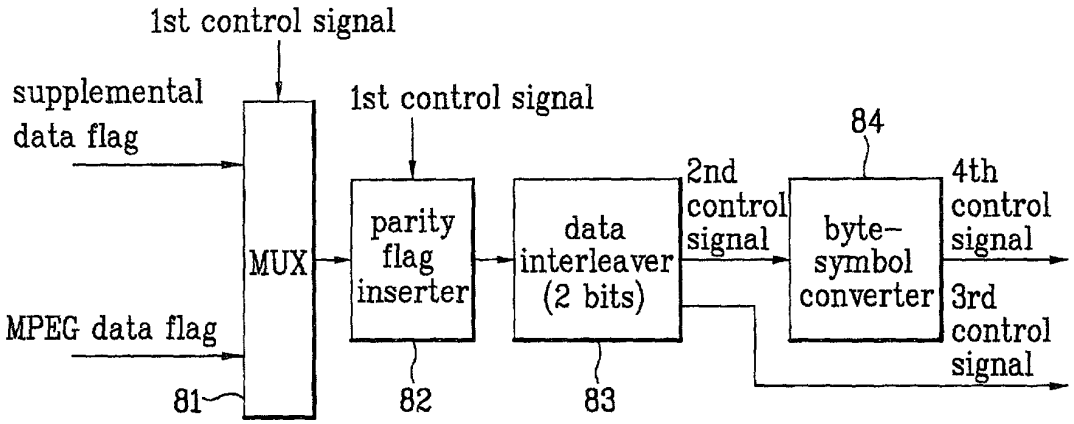
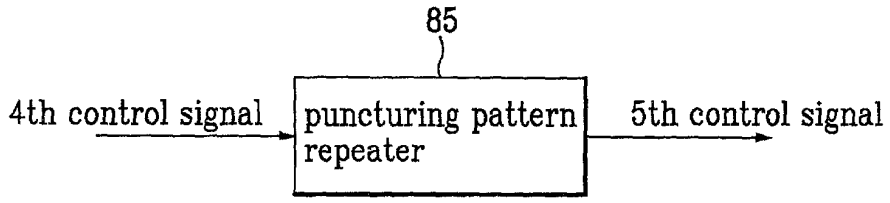

1st control signal
supplemental data flag
MPEG data flag
MUX
81
1st control signal
parity flag inserter
82
data interleaver (2 bits)
83
2nd control signal
84
byte-symbol converter
4th control signal
3rd control signal

FIG.13


85
4th control signal
puncturing pattern repeater
5th control signal